3D-CSP VERSUS OTHER PACKAGING AND ASSEMBLY TECHNOLOGIES

The following list summarizes features explicitly mentioned by other packaging and assembly companies, and it is checked if 3D-CSP fulfills them or allows improvements.

Feature	State of the art on the market	Feature implemented by 3D-CSP
Strategic features		
Batch packaging approach	Irvine-Sensors and 3D-PLUS based on neo-wafer level integration (“rebuilt wafers”)	Yes
Serial process needed for chip interconnection	Wire bonding is a typical process for die stacking (e.g. AMKOR) Also expensive laser ablation processes are used to disjoin metalized	3D-CSP uses batch oriented metallization and micro structuring approach to avoid serial processes
Generation of package and housing	Usually molding required involving tooling costs. Package and housings are made separately	Simple, without-tooling approach Integrated approach, package and housing are the same component, no extra efforts
Integration of different silicon technologies in one package	yes, depending on stacking procedure	Yes
Orthogonal arrangements of dies (e.g. for accelerometers)	Complicated arrangement	Yes, “Brick in the box” method
Integration of heterogeneous components to give, e.g., autarkic Microsystems	Depending of methods used	Yes
Perspective for further miniaturization of the SiP	fair	Excellent

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Component features		
Thinned dies needed	Yes for die stacking (e.g. AMKOR)	Any thickness can be integrated
Bond pad size	50 µm x 50 µm	20 µm x 20 µm
Bond pads everywhere on the chip	No, usually at the edges	Yes
Overhang chips	Yes	Yes
Integration of passives	Yes, e.g. Irvine Sensors, 3D-Plus	Yes, 0201 SMD components possible
Integration of non-electrical components	Yes, depending of methodology	Yes
die to die signal routing	Yes	Yes
Tile height		Defined by the height of the highest component
dam and fill capability	Partly available	not needed
Coil integration		Coils for, e.g. RF and transponder applications are seamlessly integrated
System features		
Package sizes	3x3 mm for die stacking (AMKOR)	Depending on the largest component only
Max. number of dies stacked	5-9 (e.g. AMKOR)	No real limit
Metallization planes for cooling or EMC/EMI	Yes, depending of methodology	Yes
microfluidic cooling channels	Not found yet	Yes
Each tile can be a SIP	Yes, depending of methodology	Yes
Each tile fully tested	Depends on the mythology	Yes
Electrical test on each level before stacking	Yes, depending of methodology	Yes

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