White Paper:
Reliability of RMPD® and 3D-CSP based packaging solutions

Introduction

The use of powerful and inexpensive manufacturing processes for high density packaging has a significant share in the success of a product. The requirements are particularly high in the micro-systems engineering sector, because components of the most varied technologies have to be integrated hybrid in smallest space. Examples are microchips with digital or analogue functions or different manufacturing technologies, RF-components, different substrate materials, SMT components, micro-lenses, micro-sensors, micro-optics, micro-mechanics etc. In microelectronics the talk is often of a “System in a Package - SiP” if, for example, the system contains a microprocessor and memory components and, as an enclosed unit, has an interface to the outside world.

The RMPD®-processes together with the 3D-CSP-process enable the development and production of SiP products, which integrate different components in the smallest space, quickly and inexpensively. The processes are quick and inexpensive firstly as a result of parallel manufacture of the packages, but also because there is no need for expensive tools (as in injection moulding or 3D-MID).

The production method of the 3D-CSP package is to build-up a solid plastic package based on an additive manufacturing technology principle. A liquid monomer or oligomer and a UV-curing process (RMPD®-process) are used to generate solid plastic parts. This part can simultaneously act as a “substrate” and also as a final housing if needed. Taking advantage of the RMPD®-process feature to integrate discrete components into built cavities or to generate electrical interconnects between the components using a metallization and micro-structuring approach, the whole package is provided with all functions needed. In summary, the plastic package can integrate electrical, optical, biological, chemical and micro-fluidic functions and generates the ready-to-use end-user product.

In this document a case study is presented for an application in the field of industrial electronics, where an analogue sensor, an amplifier and other electronic components are integrated in smallest space. The steps from the design to the final component, including reliability testing, are addressed.

Case study

The design, as shown in Figure 1, integrates in smallest space:

- 2 sensors (bare dies)
- 1 analogue signal amplifier
- 2 SMD resistors, size 0201
- 5 capacitors, sizes 0201, 0402, 0603.

The components are stacked in two component layers. The top side provides an opening to interface the outside world, the bottom side offers a Ball Grid Array (BGA), according to a

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customer specific standard, with a total of 14 contact pads, to be assembled via an RoHS compliant soldering method.

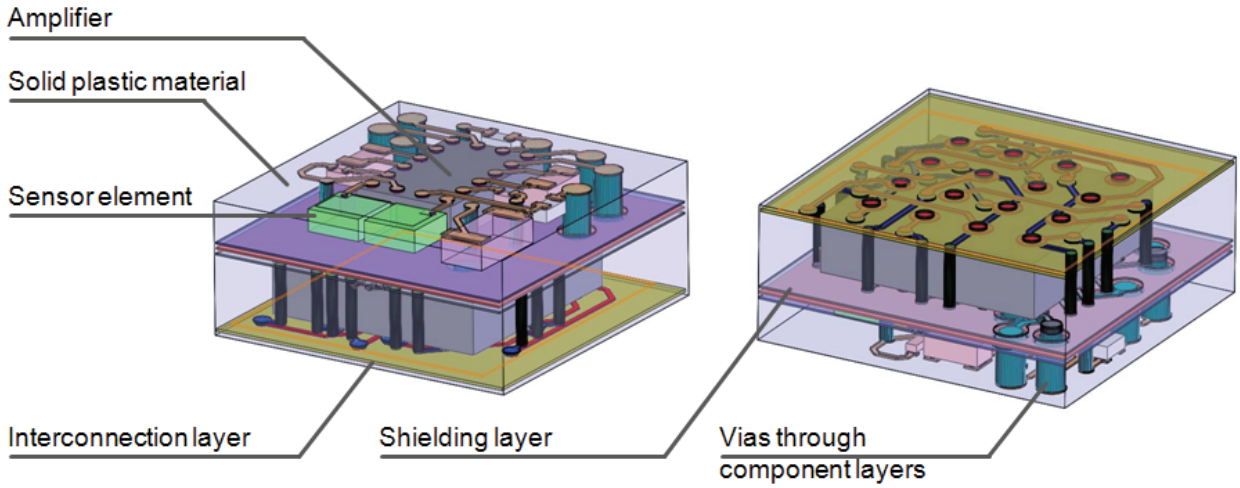
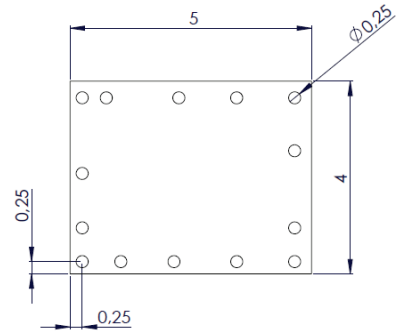


Figure 1: 3D design of a sensor package: Top view (left) and bottom view (right)

Figure 2 provides more details on the package interface.



- Package outline: 4,0 mm x 5,0 mm
- Package height: 0,8 mm
- Size tolerances < 10 µm
- Customer specific BGA
- Surface metallization: copper, gold, tin
- Ball diameter = 0,25 mm

Figure 2: Package dimensions and interface specification

The design has been implemented using microTEC's sequential built-up packaging and assembly processes (RMPD® and 3D-CSP). They work in a batch oriented way, i.e., many packages are built at the same time.

During the development phase, a multi-layer 5" mask is used to build first sample packages. Those samples are used by the customers for validation purposes, e.g., to check the electrical performance of their new electrical designs, but also to integrate them into larger systems and demonstrate - in this case - the performance of the sensor package.

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Figure 3 presents the packaged component, both from the top and bottom side.

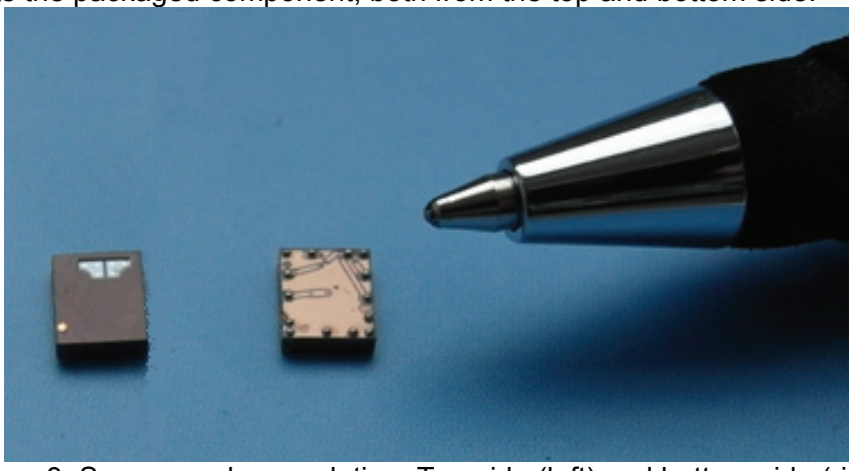

Figure 3: Sensor package solution: Top side (left) and bottom side (right)

After a successful demonstration of the packages reliability studies are being done. This includes the production of more packages. In general a new multi-layer mask is produced, which may include design optimizations, but also is of larger size, e.g., 9 inch or 14 inch. The large size allows the production of more components in parallel, so that a sufficient number of packages are produced, in short time, for extensive reliability studies. Those studies are often related to either the well-known JEDEC standards, but more often to customer specific requirements. The reason for customer specific testing is often due to the fact, that JEDEC like testing is not suitable for a component, since optics, microfluidics, micro-mechanical structures etc. might be destroyed.

For the package described temperature cycles were run, i.e., the packages were exposed to the following scheme: **1 hour at +80°C, 1 hour at -20°C**. As shown in the table below the customer validated all functions needed for the project.

	Criteria	**Cycle 0**	**Cycle 1**	**Cycle 9**	**Cycle 32**	**Cycle 58**
Current input	Current through R	1.2 mA	1.2 mA	1.2 mA	1.2 mA	1.2 mA
Channel A1	Signal shape + current level	OK	OK	OK	OK	OK
Channel A2	Signal shape + current level	OK	OK	OK	OK	OK
Trigger signal	Threshold achieved	OK	OK	OK	OK	OK
Communication	Signals received	OK	OK	OK	OK	OK

References:
microTEC design rules, s. download section at www.microTEC-d.com

Disclaimer

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